

Applicant has added the limitations of claims 14 and 15 into claim 1, amended the language of the remaining amended claims for consistency, and provided arguments distinguishing the present invention from Pathakis and Krueger.

5 **35 U.S.C. §102(b), Claim 1 Anticipation by Pathakis**

1. *Applicants have amended claim 1 to include the limitations of claims 14 and 15, thus making the anticipation rejection moot.*

The present amendment to claim 1 combining limitations from claims 14 and 15 renders the 35 U.S.C. §102 anticipation rejection moot. Applicants address the
10 Pathakis reference in the Obviousness section below.

35 U.S.C. §103(a), Claims 2-16 (and amended claim 1) Obviousness over Pathakis in view of Krueger

2. *The combination of Pathakis and Krueger do not teach that a complete
15 persistent configuration for a function, terminal, or cards of a terminal is always available and stored in a storage area of a permanent memory.*

Applicants have amended claim 1 to include limitations of claims 14 and 15 and to further clarify the scope of the invention. The invention addresses the following problem. A computer/networking system comprises numerous elements (cards,
20 boards, etc.) that require initialization data. When a system starts up or resets, initialization data for a particular element must be available so that the element can operate properly. This data must be stored in permanent memory so that in the event of a power loss or some other event that would tend to disrupt non-permanent (volatile) memory, this configuration data remains available.

25

When making changes to this configuration data however, the process for updating the configuration data may get interrupted, resulting in corrupted configuration data. The inventive database thus alternately writes this persistent configuration data to different storage areas of the permanent memory, thus assuring that there is at least one valid and uncorrupted complete configuration for the computer/networking element.

Pathakis--The Pathakis reference does teach the storage of persistent data packets in non-volatile memory, but relates to identification, handling, etc. of packets of information that are transferred between processes on computers or between databases or applications, i.e., in a communications context. It does not, however, teach or suggest the permanent storage of configurations for elements of functions, characteristics of a terminal and cards of a terminal in two separate storage areas in an alternating manner, this alternating mechanism assuring the persistent availability of an uncorrupted complete configuration data packet as provided by the amended claim language.

Krueger—The Examiner appears to be citing Krueger for the proposition that a Flash Erasable Programmable Read Only Memory Chip (FEPRM) can be used as one type of non-volatile memory store, and that it would be obvious to use such a device in the present invention. Applicants do not disagree with the assertion that it is obvious to use an FEPRM for certain types of non-volatile memory storage.

Nonetheless, Krueger does not teach or suggest the element of amended claim 1 missing from Pathakis that Applicants have identified above, namely the use of two storage areas that are alternately written to for storing complete configuration information for one of the entities defined by claim 1, thus ensuring that a complete configuration is available.

Since neither of these references, either alone or in combination, teach or suggest the elements of amended claim 1, Applicants assert that the present amendment to claim 1 distinguishes the invention from the art cited against it, and respectfully request that the Examiner withdraw the 35 U.S.C. §§102 and 103 rejections
5 against it.

Conclusion

Inasmuch as each of the rejections have been overcome by the amendments and arguments presented, and all of the Examiner's suggestions and requirements have been satisfied, it is respectfully requested that the present application be
10 reconsidered, the rejections be withdrawn and that this application be passed to issue.

Respectfully submitted,

 (Reg. No. 45,877)
15 Mark Bergner
SCHIFF HARDIN & WAITE
PATENT DEPARTMENT
6600 Sears Tower
Chicago, Illinois 60606-6473
20 (312) 258-5779
Attorney for Applicants
Customer Number 26574

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United
25 States Postal Service as First Class Mail in an envelope addressed to: Assistant
Commissioner for Patents, Washington, D.C. 20231 on August 31, 2001.


30 Mark Bergner Attorney for Applicants

**APPENDIX A
MARKED UP CLAIMS**

1. (Amended) A data base for storing persistent [permanent] data, comprising:
a buffer into which is written persistent [all] data to be permanently stored;

5 a permanent memory connected to the buffer, the permanent memory having at least two storage areas, into [in each of] which the persistent [all permanent] data is alternately written, [from the buffer is stored] each storage area being structured to store a complete permanent configuration for at least one of: a) functions, b) characteristics of a terminal and, c) cards of the terminal, at least one of the permanent configurations
10 stored having a complete configuration available and being selected for hardware implementation.

2. (Amended) The data base according to claim 1, wherein the data base further comprises a control mechanism within a first application process for management of a
15 first memory controls writing of the data to be persistently [permanently] stored into the buffer, the data being generated or modified by the first application process alone or also by other application processes running simultaneously with the first application process.

20 3. (Amended) The data base according to claim 2, wherein for a number of application processes running simultaneously, a control mechanism within the first application process, by exchanging messages with control mechanisms of the other application processes, controls accesses, required for loading the data to be persistently [permanently] stored, of individual application processes running
25 simultaneously, to the buffer using process identification numbers, entered in a shared memory, of the application processes running simultaneously.

4. (Amended) The data base according to claim 1, wherein all of the persistent [permanent] data stored in the buffer is alternately written into one of the storage units or storage areas of the permanent memory.

5

8. (Amended) The data base according to claim 1, wherein only the persistent [permanent] data, if necessary including reconstruction data, is transferred into the buffer from a first memory which contains a run-time program and associated permanent data.

10

9. (Amended) The data base according to claim 8, wherein the persistent [permanent] data is stored in a space-saving manner as a data sequence in the buffer and in the permanent memory.

15

10. (Amended) The data base according to claim 1, wherein at least one further permanent memory is provided for a start program and application software including data base management software, with use of which configuration data to be written into the first memory is automatically reconstructed from the persistent [permanent] data stored in the permanent memory.

20

12. (Amended) The data base according to claim 1, wherein the buffer has at least two random access memories, functionally connected in series, persistent [permanent] data stored in the first random access memory being written into the second random access memory so that the first random access memory is available for reloading while persistent [permanent] data from the second or a further random access

25

memory is written into the permanent memory.

16. (Amended) The data base according to claim 1 [14], wherein a number of configuration changes are only performed at a data management side and thereafter at
5 least one of a functional and a [/or] hardware change comprising all configuration changes is performed in the terminal.